CLAIMS

What is claimed is:

1. A method for encoding instructions as a very long instruction word for processing in a plurality of computation units that reduces instruction memory requirements in a processing system, the method comprising the steps of:

(a) determining at which stages of instruction processing that an instruction code needs to be executed; and

(b) utilizing an enable signal of the instruction code to direct execution during the determined stages by enabling storage operations for the instruction code.

2. The method of claim 1 where the instruction code is associated with one of a plurality of computation units.

3. The method of claim 2 further comprising the step of (c) utilizing an action signal of the instruction code to execute each instruction when.

4. The method of claim 3 wherein utilizing an enable signal step (b) further comprises the step of (b1) encoding a chosen number of bits of the instruction code as the enable signal.

5. The method of claim 4 wherein the utilizing an action signal (c) further comprises the step (c1) encoding a remaining number of bits of the instruction code as the action signal.

6. The method of claim 3 wherein utilizing the enable signal and action signal for the instruction code avoids utilizing NOP (no operation) instruction codes in the very long instruction word.

7. A method for forming a very long instruction word in a processing system, the method comprising the steps of:

(a) encoding each instruction code of the very long instruction word as an enable signal and an action signal to collapse instruction fields in the very long instruction word; and

(b) associating each instruction code with a computation unit.

8. The method of claim 7 further comprising the step of (c) utilizing the enable signal to control storage operations when the action signal of each instruction is processed in the computation unit.

9. The method of claim 8 wherein the utilizing the enable signal (step c) occurs during each stage of processing.

10. The method of claim 9 wherein the utilizing the enable signal step (c) occurs during a loop stage of processing.

11. The method of claim 7 wherein the associating step (b) further comprises the step of (a1) associating based on a dataflow graph.

12. The method of claim 7 wherein the encoding step (a) further comprises the step of (a1) scheduling the very long instruction word for parallel processing.

13. A system for encoding instructions as a very long instruction word for processing that reduces instruction memory requirements in a processing system, the system comprising:

a plurality of computation units; and

a controller for controlling the plurality of computation units, wherein the controller determines at which stages of instruction processing that an instruction code needs to be executed and utilizes an enable signal of the instruction code to direct execution during the determined stages by enabling storage operations for the instruction code.

14. The system of claim 13 wherein the controller further utilizes an action signal of the instruction code for execution of each instruction in one of the plurality of computation units.

15. The system of claim 14 wherein the controller further encodes a chosen number of bits of the instruction code as the enable signal.

16. The system of claim 15 wherein the controller further encodes a remaining number of bits of the instruction code as the action signal.

17. The system of claim 13 further comprising an adapatable computing engine, the adaptable computing engine including the plurality of computation units and the controller.